

## Patent Claims

1. A patterning method,  
in which the following method steps are performed:
  - 5 application of an auxiliary layer (14, 14c) to a carrier material (12, 10c),  
patterning of the auxiliary layer (14, 14c) and of the carrier material (12, 10c) with production of a cutout (18, 18c),
  - 10 expansion of the cutout (18, 18c) in the region of the auxiliary layer (14, 14c), the cutout (18, 18c) in the region of the carrier material (12, 10c) not being expanded or not being expanded to as great an extent as in the region of the auxiliary layer (14, 14c),
  - 15 filling of the expanded cutout (18b, 18d) with a filling material (22, 22c),  
removal of the auxiliary layer (14, 14c) after filling,  
patterning of the carrier material (12, 10c) using the filling material (22, 22c) and with production of at  
20 least one further cutout.
2. The method as claimed in claim 1, characterized by the following steps:
  - 25 application of a mask layer (16, 16c) to the auxiliary layer (14, 14c) prior to the production of the cutout (18, 18c),  
patterning of the mask layer (16, 16c) by means of a lithographic method,  
production of the cutout (18, 18c) in accordance with  
30 the patterned mask layer (16, 16c).
3. The method as claimed in claim 1 or 2, characterized by the following step:
  - 35 planarization of the filling material (22, 22c) prior to the repeated patterning.
4. The method as claimed in one of the preceding claims, characterized in that it is used for producing

a minimum feature size of less than one hundred nanometers or less than fifty nanometers.

5. The method as claimed in one of the preceding  
5 claims, characterized by the following steps:  
formation of a mask layer (12) as carrier material  
prior to the application of the auxiliary layer (14),  
patterning of a basic material (10) using the mask  
layer (12) after the patterning of the carrier material  
10 (12) using the filling material (22).

6. The method as claimed in one of the preceding  
claims, characterized by the following step:  
use of a semiconductor material (10c) as carrier  
15 material (10c), in particular a monocrystalline  
semiconductor material (10c).

7. The method as claimed in claim 6, characterized by  
the following step:  
20 formation of at least one layer (50, 52) in the  
expanded cutout (18d) prior to filling, in particular  
of an electrically insulating layer (50) and of an  
electrically conductive layer (52).

8. The method as claimed in claim 7, characterized in  
that the layer (50, 52) is patterned by a method as  
claimed in one of claims 1 to 5.

9. The method as claimed in one of claims 6 to 8,  
30 characterized by the following steps:  
filling of the further cutout with a further filling  
material (70),  
removal of the filling material (22, 22c) serving for  
patterning after the filling of the further cutout.

35 10. The method as claimed in one of claims 6 to 8,  
characterized by the following steps:

partial removal of the filling material (22, 22c) from the cutout (18, 18c), one part of the bottom of the cutout (18, 18c) being uncovered and another part of the bottom of the cutout (18, 18c) remaining covered  
5 with filling material (22, 22c).

11. The method as claimed in one of claims 6 to 10, characterized by the following step:  
oxidation of the semiconductor material (10c) in the  
10 region between the cutout (18c) and the further cutout, in particular in an intermediate region extending from the cutout (18c) to the further cutout, preferably prior to the removal of the filling material (22c) and preferably after the production of an  
15 oxidation protective layer (80) on at least one sidewall of the further cutout.

12. A field effect transistor (100),  
having two channel connection regions (104, 106),  
20 having a control region (52, 62) containing at least two control sections,  
having an active region (56) arranged between the channel connection regions (104, 106), on the one hand, and between two control region sections, on the other  
25 hand,  
and having insulating regions (50, 60) that are electrically insulating and are arranged between the control region sections and the active region (56),  
characterized by at least two further control region  
30 sections contained in the control region (52, 62),  
by a further active region (56) arranged between the channel connection regions (104, 106), on the one hand, and between two further control region sections, on the other hand,  
35 and by further insulating regions (50, 60) that are electrically insulating and are arranged between the further control region sections and the further active region (56).

13. The field effect transistor (100) as claimed in claim 12, characterized by a substrate (10c), in which the field effect transistor (100) is formed,  
5 the active regions being formed in projections (56) of the substrate (10c).

14. The field effect transistor (100) as claimed in claim 13, characterized in that the channel connection  
10 regions (104, 106) are at the same distance from the bottom of a trench (18c) arranged between two projections (56).

15. A field effect transistor (100),  
15 having two channel connection regions (104, 106), having a control region (52, 62) containing at least two control region sections, having an active region that is formed as a projection (56) of a substrate (10c) and is arranged between the  
20 channel connection regions (104, 106) on the one hand, and between two control region sections, on the other hand, and having insulating regions (50, 60) that are electrically insulating and are arranged between the  
25 control region sections and the active region (56), characterized in that the projection (56) is isolated from the substrate (10c) at its base by an insulating material (82) that is electrically insulating.

30 16. The field effect transistor (100) as claimed in claim 15, characterized in that two side areas of the projection (56) that lie at the base of the projection transversely adjoin two substrate areas of the substrate (10c) that are arranged in two planes spaced  
35 apart from one another, the distance (D) being greater than one nanometer, greater than three nanometers or greater than five nanometers.

17. The field effect transistor (100) as claimed in claim 15 or 16, characterized in that the control region sections are formed on the two side areas of the projection (56).

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18. The field effect transistor (100) as claimed in one of claims 15 to 17, characterized in that the insulating material (82) ends laterally at the projection (56) and, in particular, does not project  
10 beyond at least one side area of the projection (56).